or alloys thereof. Certain TFT arrays may include other components, such as storage-capacitors, and as such, the extra components will likely utilize electrodes which can be formed during this process as well.

[0042] Referring to FIG. **1**C, a dielectric layer **109** is formed over the surface of the substrate and particularly over the electrodes **105** and **107**. Formation of the dielectric layer **109** is generally undertaken to facilitate the appropriate capacitance and electronic responses between the gate electrode the semiconducting layers. In particular, the forming the dielectric layer **109** can include a deposition process, such as a thin film deposition process, and particularly a chemical vapor deposition (CVD) process, physical vapor deposition (PVD) (e.g., sputtering), atomic layer deposition (ALD), or any combination thereof. In one particular embodiment, the dielectric layer **109** is formed via plasma-enhanced CVD (PECVD).

[0043] In one such embodiment, the dielectric layer **109** includes a dielectric material, having a dielectric constant of greater than about 2.0. According to one embodiment, the dielectric layer **109** includes a material having a dielectric constant of not less than about 4, such as not less than about 6, or even, not less than about 8. In one embodiment, the dielectric layer **109** includes a nitride or an oxide, or a combination thereof. Suitable nitrides can include silicon nitride (e.g., SiN_x), which is directly deposited over the gate electrodes. Other embodiments utilize an oxynitride, such as SiO_xN_y. Generally, the dielectric layer **109** has a thickness of not greater than about 600 nm, and particularly within a range between about 200 nm and about 500 nm.

[0044] Referring to FIG. **1**D, a cross-sectional view of the workpiece of FIG. is illustrated after forming a portion of the semiconducting region **110**. Notably, formation of the semiconducting regions **110** can include a masking and patterning step such that the semiconducting regions are properly placed and deposited in relation to the gate electrodes, bus lines, and other electrodes. In particular, the forming the intermediate layer **111** can include a deposition process, such as a thin film deposition process, and particularly a chemical vapor deposition (CVD) process, physical vapor deposition (PVD) (e.g., sputtering), atomic layer deposition (ALD), or any combination thereof. In one particular embodiment, the intermediate layer is formed via plasma-enhanced CVD (PECVD).

[0045] The intermediate layer **111** generally includes a semiconducting material. The intermediate layer **111** includes a semiconductor material such as silicon, germanium, carbon, another semiconductor material, such as a III-V or a II-VI material, or any combination thereof. According to a particular embodiment, the intermediate layer **111** includes silicon, and particularly amorphous silicon (a-Si). The intermediate layer **111** can be undoped, or alternatively the intermediate layer **111** can be doped. In another embodiment, the intermediate layer **111** includes either fully or partially depleted n-type active semiconductor region, p-type active semiconductor region, or any combination thereof. The intermediate layer **111** has a substantially uniform thickness, generally having an average thickness of not greater than about 500 nm, and particularly within a range of about 50 nm to about 400 nm.

[0046] In further reference to the semiconducting region, FIG. **1**E illustrates a cross-sectional view of the workpiece of FIG. **1**D after forming a top semiconducting layer **113** overlying the intermediate layer **111**. In one embodiment, the top semiconducting layer **113** is formed via a deposition process, such as a thin film deposition process, and particularly using chemical vapor deposition (CVD), physical vapor deposition (PVD) (e.g., sputtering), atomic layer deposition (ALD), or any combination thereof. In one particular embodiment, the top semiconducting layer **113** is formed via plasma-enhanced CVD (PECVD).

[0047] The top semiconducting layer **113** can include a semiconducting material, such as silicon. According to one embodiment, the top semiconducting layer **113** includes a doped semiconducting material, such as a doped amorphous silicon, and particularly n-type doped amorphous silicon. Generally, the top semiconducting layer **113** has a thickness of not greater than about 3000 Angstroms, and particularly within a range between about 200 Angstroms and about 1000 Angstroms.

[0048] As will be appreciated, fewer or greater number of layers can be included in the semiconducting region **110**, depending upon the intended transistors being formed. As such, the semiconducting region **110** typically includes at least one layer including silicon, such as an amorphous silicon, polysilicon, or silicon nitride, p-type doped silicon, n-type doped silicon, and more typically any combination of layers including such materials. In forming a series of layers, the process can further include a series of etching steps to properly remove portions of layers. Generally, the semiconducting region typically has a thickness on the order of about 300 nm to about 900 nm.

[0049] In addition to forming a semiconducting region **110**, the process of forming a TFT can include formation of a pixel region. Referring to FIG. **1**F, a cross-sectional view of the workpiece of FIG. **1**E is illustrated after forming a transparent electrode **115**. It will be appreciated that the formation of a transparent electrode can be undertaken during the formation of the semiconducting region **110**, and particularly during the formation of the multiple films within the semiconducting region **110**. Notably, the formation of the transparent electrode **115** is not part of the formation of the transistor, but rather part of the formation of a pixel that is controlled by the transistor. Formation of the transparent electrode **115** can include a patterned mask and deposition process. As such, the transparent electrode **115** can be formed via a deposition process, such as a thin film deposition process, and particularly using chemical vapor deposition (CVD), physical vapor deposition (PVD) (e.g., sputtering), atomic layer deposition (ALD), or any combination thereof.

[0050] Generally, the transparent electrode **115** is substantially transparent to a particular spectrum of radiation, such as visible light. Moreover, the transparent electrode **115** is particularly thin, and generally has an average thickness within a range between about 10 nm to about 100 nm. Moreover, the transparent electrode material is a conductive or semiconductive material, particularly a substantially transparent material. Suitable transparent, conductive or semiconductive materials can include oxides, such as metal oxides, and particularly indium tin oxide, often referred to as ITO.

[0051] After the formation of the transparent electrode **115**, the process continues with the formation of source/drain regions for each of the gate electrodes. Referring to FIG. **1**G, a cross-sectional view of the workpiece of FIG. **1**F is illustrated after forming the source/drain portions **117**. As will be appreciated, depending upon the method of forming, forming the source/drain portions **117** can include using a patterned mask and/or etching process to properly place the source/drain portions **117** in contact with the semiconducting layers